Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

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**.042”**

**.042”**

**Chip back is Collector**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Collector**

**Geometry: G1**

**APPROVED BY:DK DIE SIZE .015” X .015” DATE: 10/5/22**

**MFG: ZETEX THICKNESS: .006” P/N: BCW72**

**DG 10.1.2**

#### Rev B, 7/19/02